



End Semester/Reappear (Semester III) Examination December, 2024

Programme: B. Tech CSE

Course: Computer Organization & Architecture

Course Code: 3PCCCS202

Enrolment no. _____

Full Marks: 70

Time: 3 Hrs.

Q. No.	Questions	CO	Bloom Taxonomy Category	Marks
Section I				
1	Short Answer type questions			4 x 5 = 20
a	Given a simple instruction like ADD R1, R2, explain the steps in the instruction execution cycle of a CPU, including fetching, decoding, and executing the instruction.	CO1	Remember	
	or			
b	Write the binary representation of the signed number -12 using two's complement notation in 8-bit format.	CO1	Remember	
	or			
c	What is the purpose of privileged and non-privileged instructions in CPU design? Provide examples.	CO2	Understand	
	or			
d	Describe the role of interrupt-driven I/O in CPU and its advantages over program-controlled I/O.	CO2	Remember	
	or			
e	Explain the difference between static and dynamic RAM with respect to their usage in memory systems.	CO3	Understand	
	or			
f	List and explain the basic functions of the different I/O device interfaces (e.g., SCII and USB).	CO3	Remember	
	or			
Section II				
Long Answer type questions				
2	Express the concept of Direct Memory Access (DMA). Explain how DMA improves system performance over program-controlled I/O and interrupt-driven I/O. Include a diagram to illustrate the data transfer process.	CO2	Understand	3 x 10 = 30
	or			
3	Design a simple hypothetical CPU with a hardwired control unit. Explain the limitations of this approach compared to a micro programmed control unit.	CO2	Create	
	or			
4	Distinguish the different types of pipeline hazards (data hazards, control hazards, structural hazards). Explain how each of these hazards can impact the performance of a pipelined processor.	CO3	Analyze	
	or			
5	Discuss the basic concept of pipelining. Explain how instruction pipelining improves CPU performance, and describe the stages typically involved in an instruction pipeline.	CO3	Remember	
	or			
6	Describe and compare the common cache replacement algorithms, such as Least Recently Used (LRU), First-In-First-Out (FIFO), and Random Replacement. How do these algorithms impact cache efficiency?	CO5	Analyze	
	or			
7	Explain the different types of cache mapping: direct-mapped, set-associative, and fully associative. What are the advantages and disadvantages of each?	CO5	Analyze	
	or			

Section III			
Application based questions			
5	Explain the concept of Booth's multiplication algorithm. Use the algorithm to multiply the decimal numbers 6 and -3, showing all the steps involved in the process.	CO1	Analyze
	or		
	Evaluate a 4-bit binary adder implemented as both a ripple carry adder and a carry look-ahead adder. Perform the addition of the numbers 9 (1001) and 5 (0101) using each circuit. Compare the propagation delays for both adders and explain why the carry look-ahead adder operates faster.	CO1	Evaluate
			1 x 20 = 20

COURSE OUTCOME

At the end of the course the candidate will able to

CO1: Draw the functional block diagram of single bus architecture of a computer and describe the function of the instruction execution cycle, RTL interpretation of instructions, addressing modes, instruction set.

CO2: Write assembly language program for specified microprocessor for computing 16 bit multiplication, division and I/O device interface (ADC, Control circuit, serial port communication).

CO3: Write a flowchart for Concurrent access to memory and cache coherency in Parallel Processors and describe the process.

CO4: Given a CPU organization and instruction, design a memory module and analyze its operation by interfacing with the CPU.

CO5: Given a CPU organization, assess its performance, and apply design techniques to enhance performance using pipelining, parallelism and RISC methodology.